# Design and Implementation of Any time Electricity Bill Payment (ATP) Machine Controller

Team Spark

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CONTENTS

[Design and Implementation of Any time Electricity bill Payment (ATP) machine controller 1](#_Toc140278097)

[I. BLOCK DIAGRAM 3](#_Toc140278098)

[II. FSM 4](#_Toc140278099)

[III. APPROACH 5](#_Toc140278100)

[IV. METHODOLOGY/FLOW 5](#_Toc140278101)

[RTL View: 6](#_Toc140278102)

[Error: 6](#_Toc140278103)

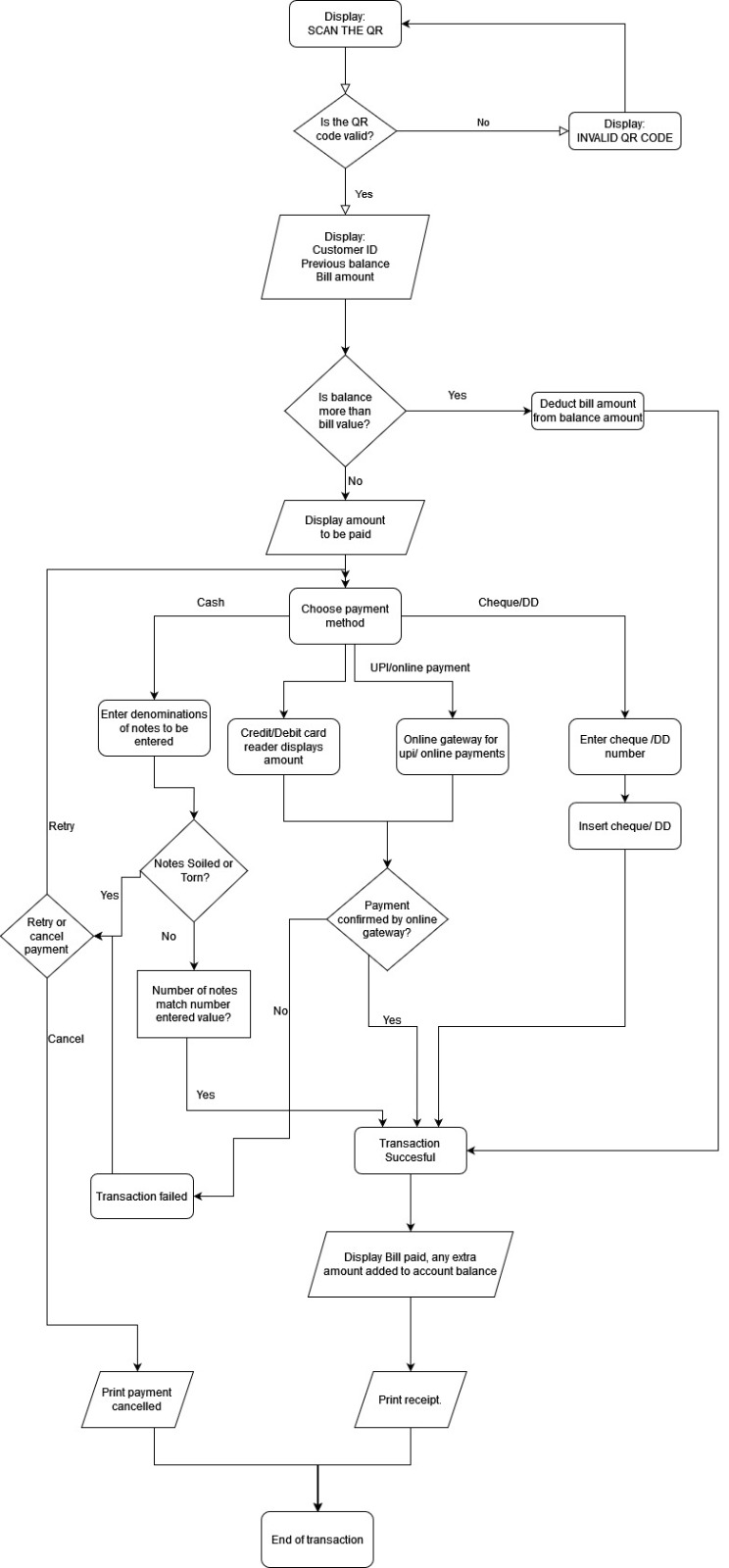
[V. GITHUB FILE SCREENSHOT 7](#_Toc140278104)

[VI. RESULTS AND SUMMARIZATIONS 7](#_Toc140278105)

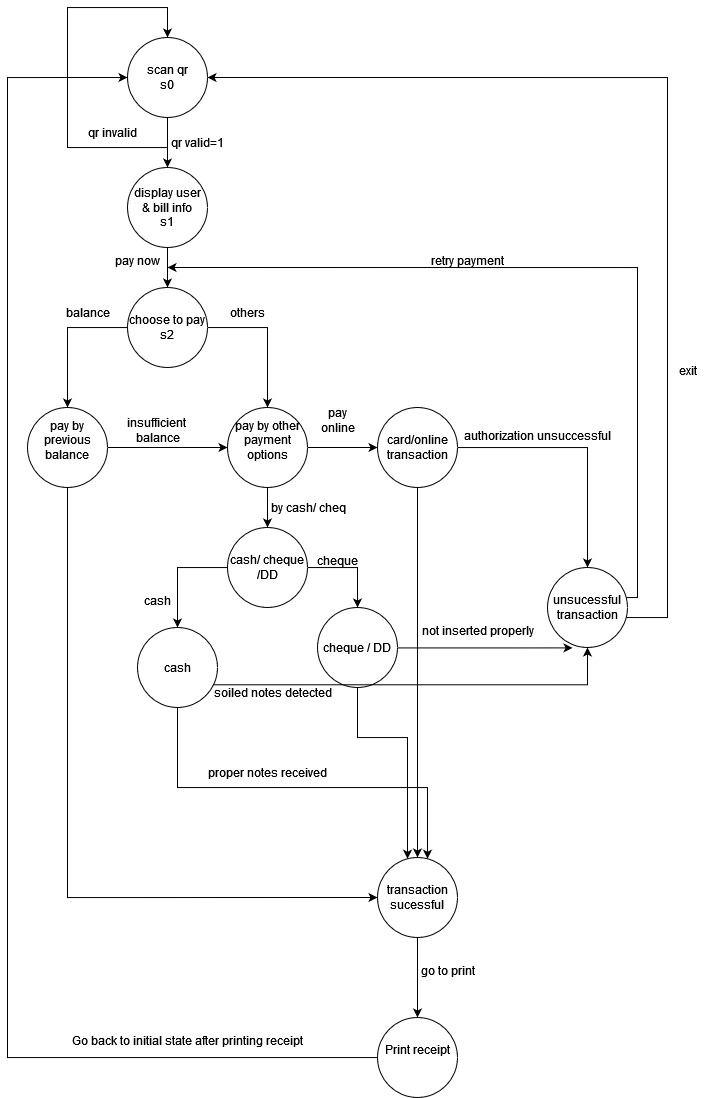
[VII. REFERENCES 7](#_Toc140278106)

In this project, we have tried to design and implement an Any Time Electricity Bill Payment (ATP) Machine Controller using FPGA.

## BLOCK DIAGRAM



# FSM



# APPROACH

1.In order to solve this problem, we drew a flowchart first which roughly summarizes our agenda and gives us a brief on methodology and how to work on it.

2. Users can pay through existing Balance, Cash, Card, Online Transactions, DD and Cheque.

3.The machine controller uses QR Scanner in order to initiate the process.

4.After the QR gets scanned, the machine controller displays Customer ID, Existing Balance, Amount to be paid and Pay option.

5.If Balance is greater than the Bill amount then the amount gets deducted automatically else the machine controller moves further and displays other payment options.

6.The machine controller displays QR for UPI payments, redirects to Online Gateway for Online payments, displays Insert DD or Cheque option for DD or Cheque and displays Insert Cash option for Cash mode of payment.

7.The machine controller does not accept soiled or torn notes.

8.If the transaction fails then the machine controller redirects to Retry Payment option.

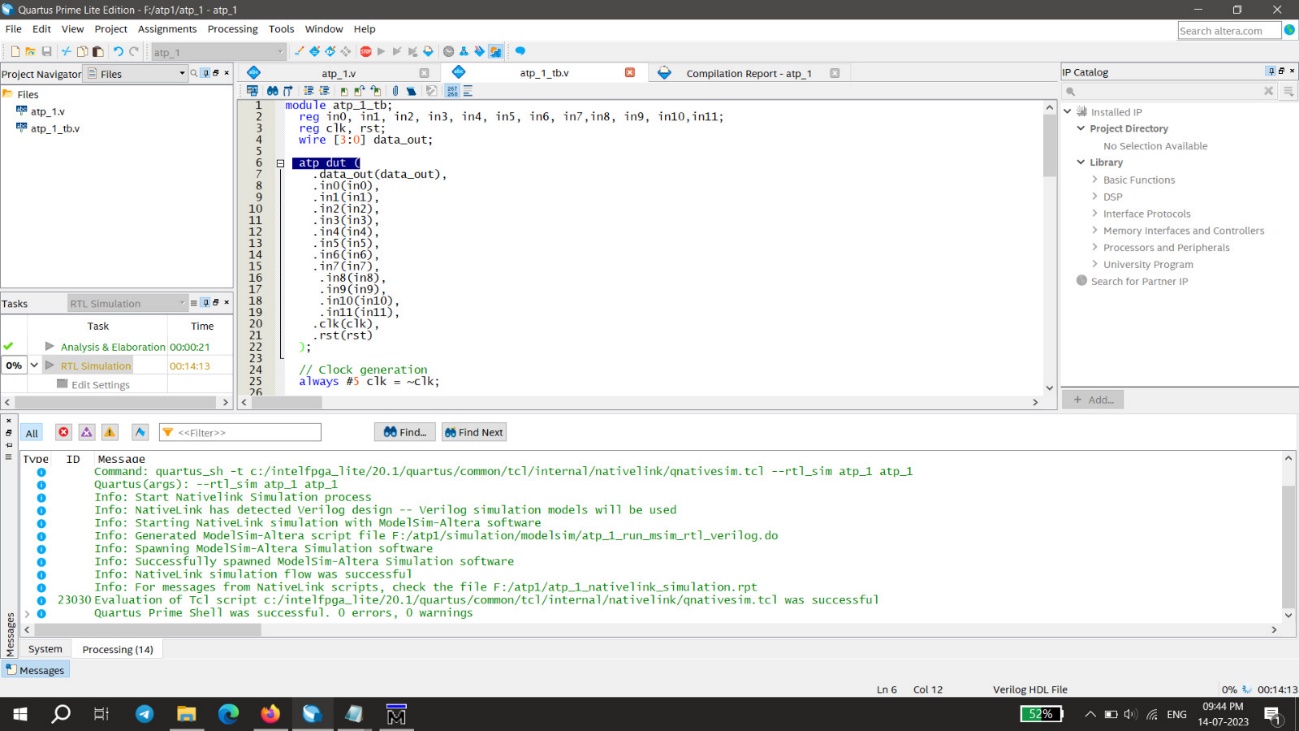
9.If the transaction is successful then the machine controller displays Bill paid successfully and Extra amount to be added option.

10. If the user wants to add balance, then the machine controller redirects the user to choose payment mode option else the receipt is printed and transaction ends.

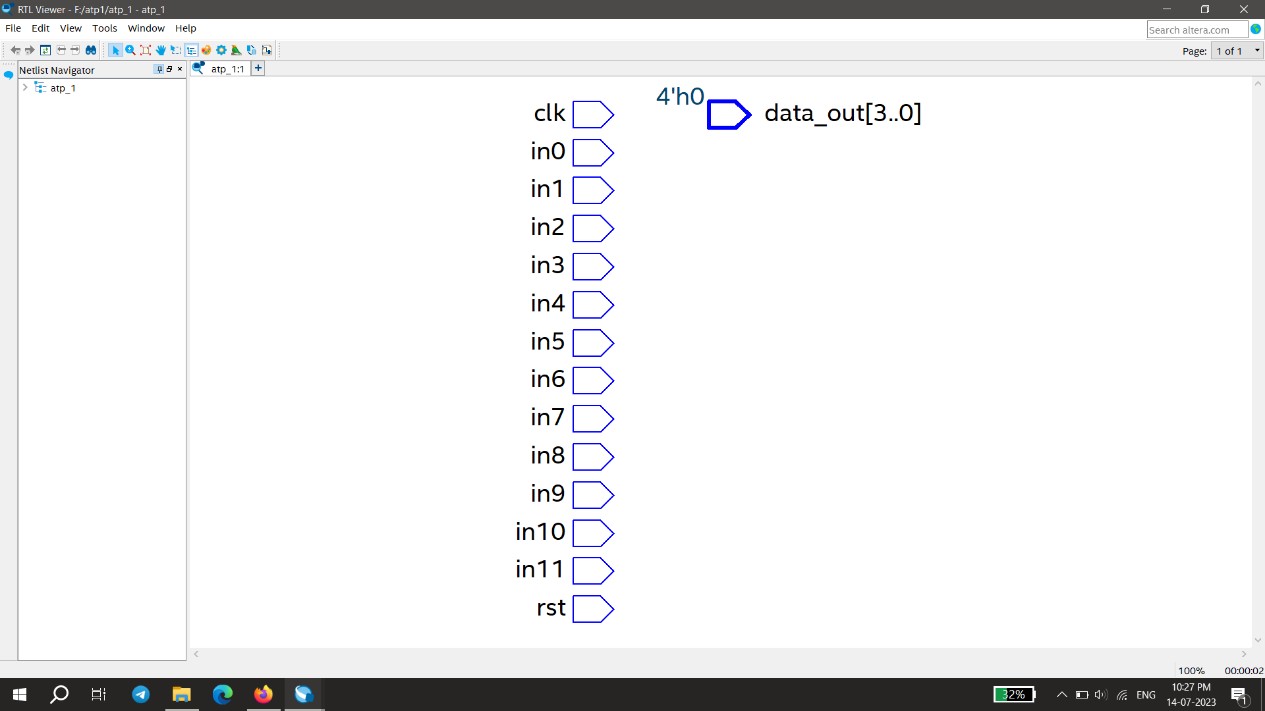
# METHODOLOGY/FLOW

1.Intel Quartus Prime Lite Software has been used to obtain results.

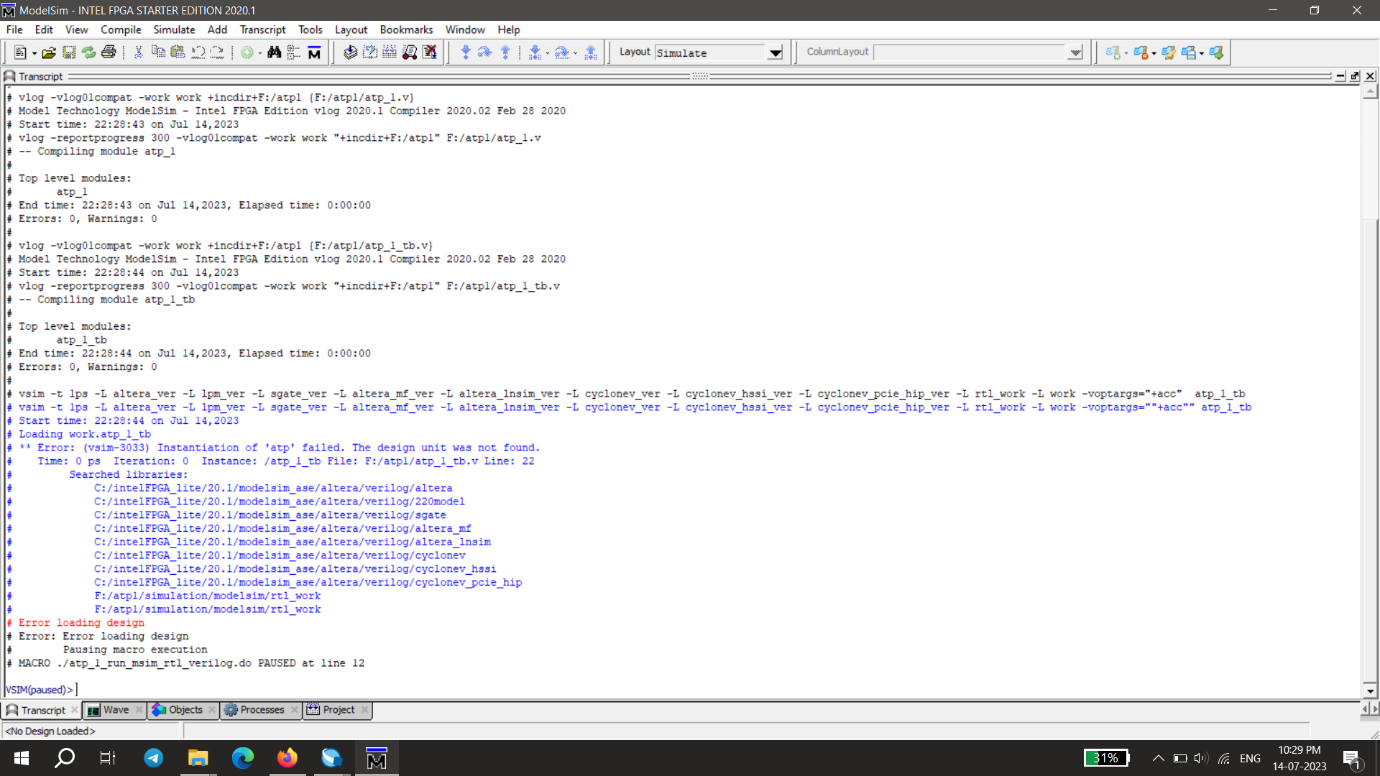
2.A Verilog HDL code and the test bench has been compiled successfully without errors to obtain the State Diagram of the given problem statement using block diagram as reference as shown in figure below.



## RTL View:

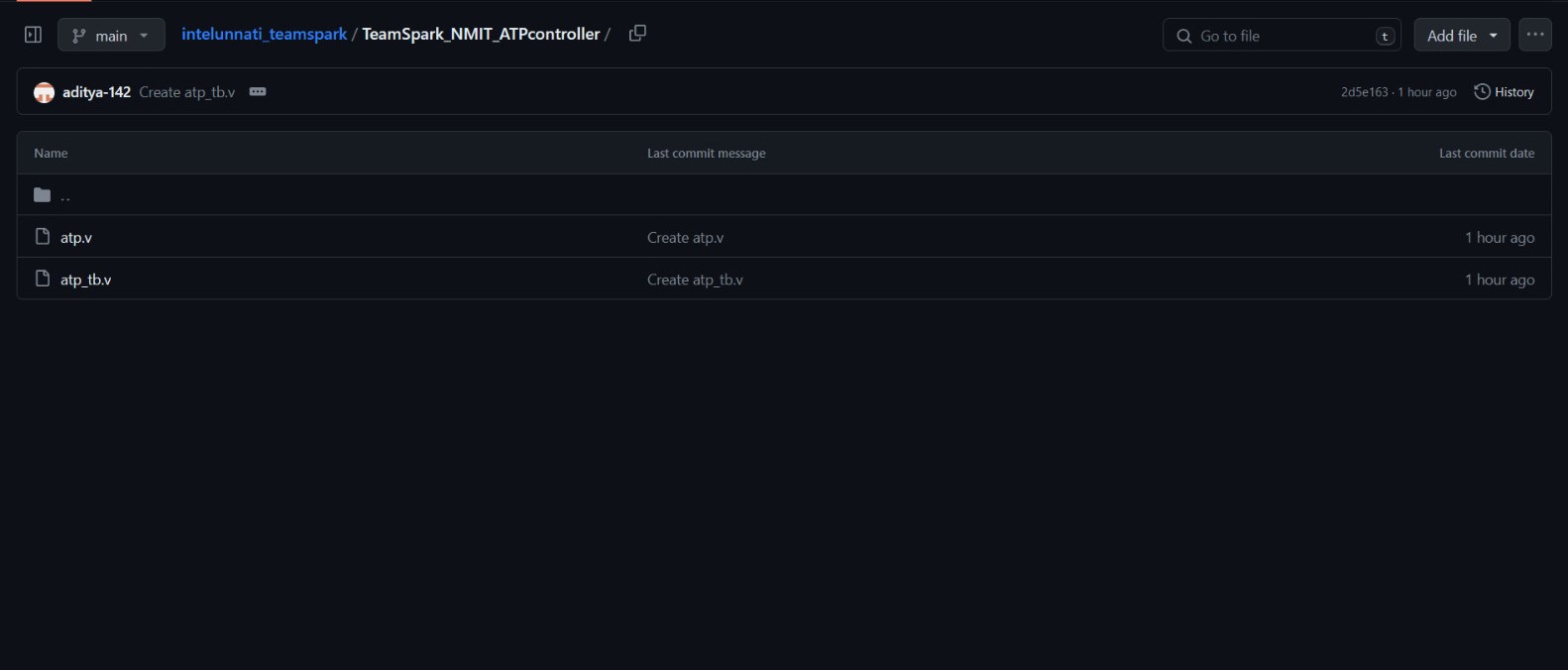


## Error:



# GITHUB FILE SCREENSHOT

GitHub Code Link: TeamSpark\_NMIT\_ATPcontroller/atp.v



# RESULTS AND SUMMARIZATIONS

The main file and the test bench have been compiled without any errors. As observed due to some technical issue the RTL simulations could not be performed. Trying to troubleshoot this issue could not be done and there was also no updated documentation for the shown error.

# REFERENCES

1.System Machine Design Techniques for Verilog HDL and VHDL.......Steve Golson

2.State Machine Coding Style for Synthesis..............Clifford E. Cummings (1998)